**Programmable Logic Devices**

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Programmable logic devices (PLDs) are integrated circuits. They contain arrays of AND and OR gates, which we can use to implement Boolean functions.

There are three types of PLDs:

1. Programmable Read Only Memory (PROM)
2. Programmable Array Logic
3. Programmable Logic Array

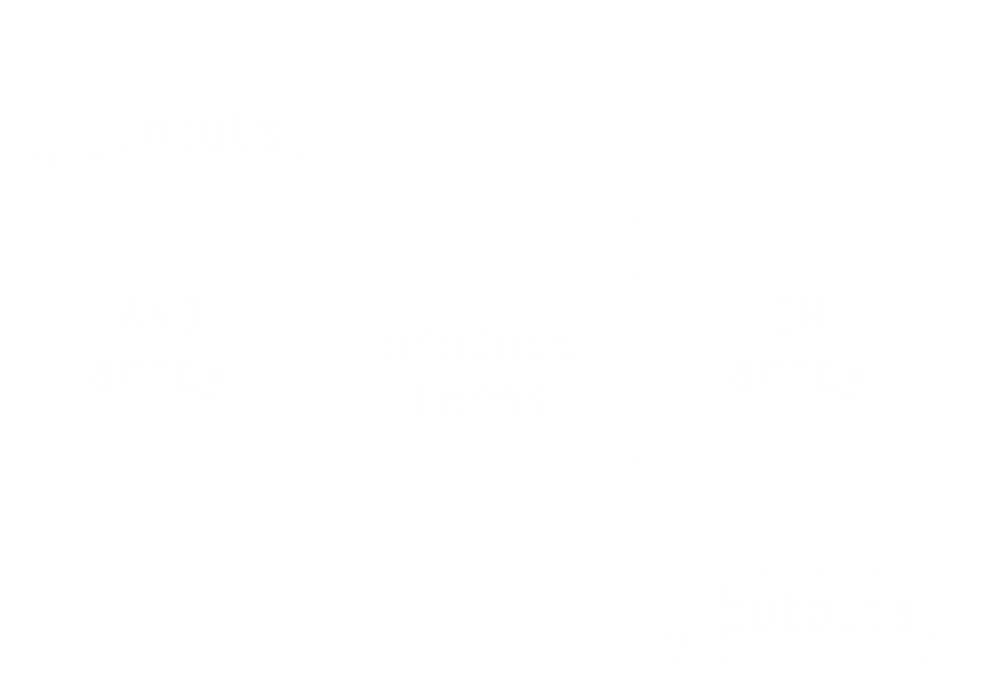
We shall not be discussing PROMs.

The process of entering information into PLDs is called hardware programming. Users can program the devices electrically to implement Boolean functions as required.

## Programmable Logic Array

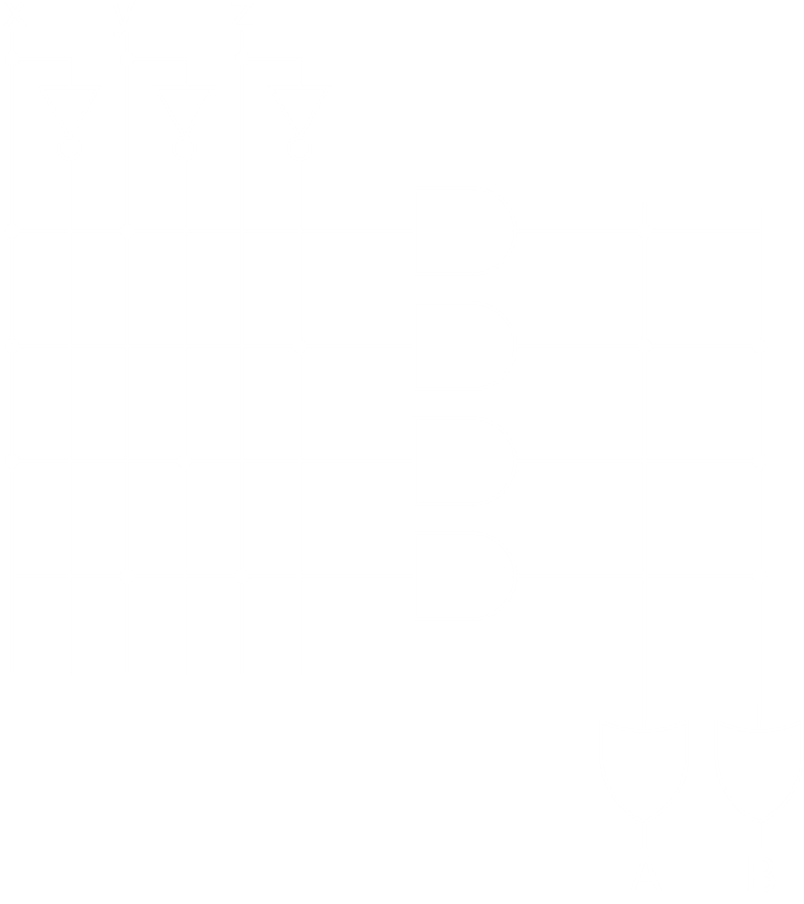
In Programmable Logic Arrays (PLAs), both the AND array and the OR array are programmable. This makes it the most flexible PLD.

Inputs are taken into the AND gate in both the normal and complemented form. Based on requirement, we can implement any combination. From the outputs of the AND gates, we can take inputs for OR gates as required. Since we are taking the outputs of the AND gates as inputs for the OR gates, the final output will be in Sum of Products (SOP) form.



Say we want to implement the following two Boolean functions:

The corresponding PLA configuration is shown below:



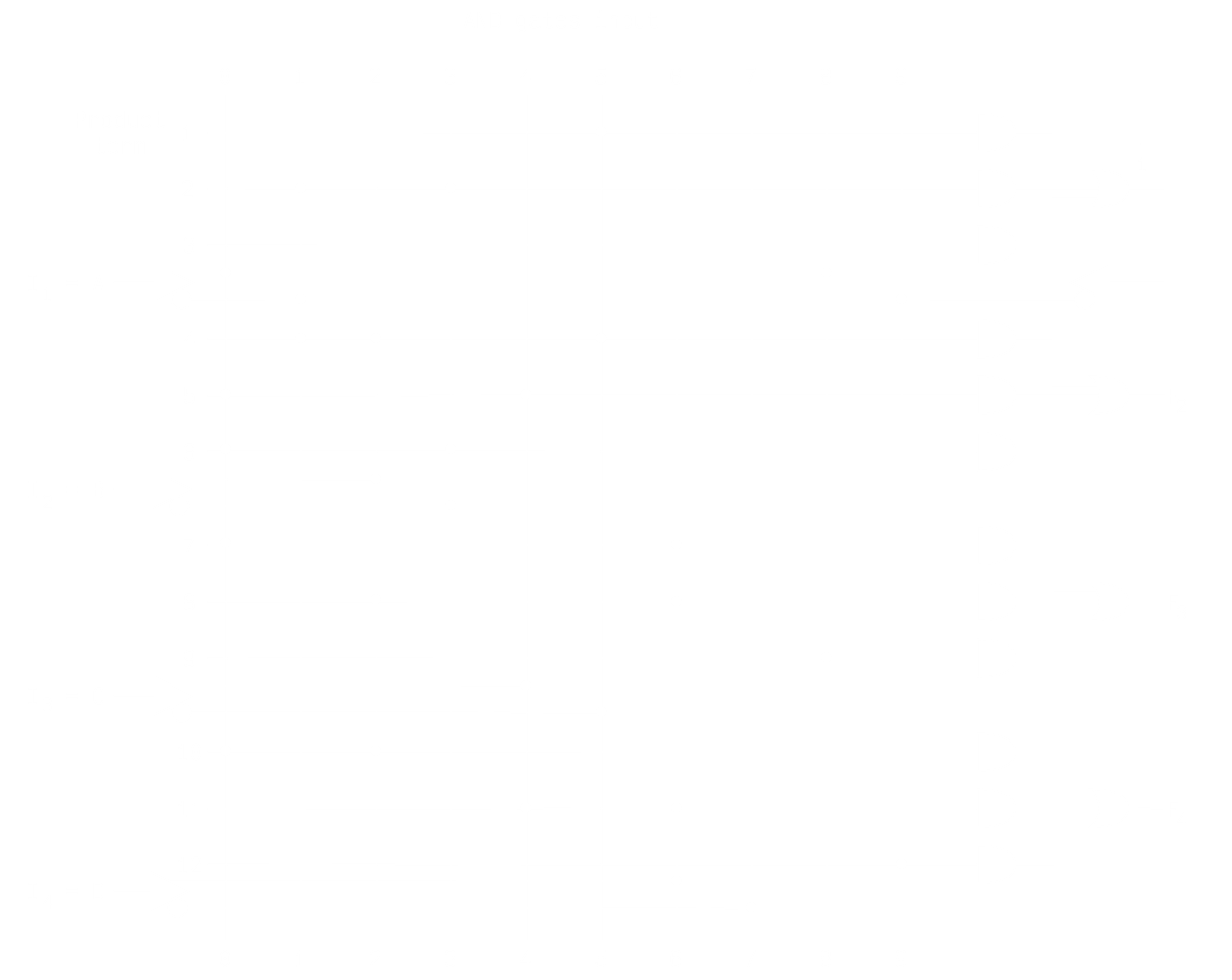
The two expressions had four different products in total, so we just needed four AND gates. Since there were two outputs, we needed two OR gates. For the inputs to the AND gates, connections were made for each of the products. For the inputs to the OR gates, connections were made for each of the sums.

## Programmable Array Logic

In programmable array logic (PAL) devices, only the AND array is programmable. The OR array is fixed by the manufacturer. PALs are easier to program and less expensive than PLAs, but they are also less flexible.

Consider the following expressions:

The PAL implementation for these equations is shown below:



There are different possible inputs, including and , so there are input lines. The OR gates are connected to three AND gates each, and we cannot do anything on that side. What we can do is configure what inputs go to each of the AND gates.

For example, for the output , we took the inputs and , which correspond to and respectively, to a single AND gate. This gave us . We took the single input to another AND gate, since we need as well. We left the third AND gate empty. The three outputs from the AND gates went to an OR gate, which gave us the output .

Further examples for different types of PLD devices can be found in the books.